RELIABILITY REPORT

FOR

MAX4582xxE

PLASTIC ENCAPSULATED DEVICES

August 6, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX4582 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4582 is a low-voltage, CMOS analog integrated circuit configured as two 4-channel multiplexers. This CMOS device can operate continuously with ±2V to ±6V dual power supplies or a +2V to +12V single supply. Each switch can handle rail-to-rail analog signals. The off-leakage current is only 1nA at +25°C or 5nA at +85°C.

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a single +5V or dual ±5V supplies.

B. Absolute Maximum Ratings

Item	Rating
Voltages Reference to V_{EE}	
V_{CC}	-0.3V to 13V
Voltage into Any Terminal (Note 1)	(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Continuous Current into Any Terminal	±20mA
Peak Current, X_, Y_, Z_ (pulsed at 1ms, 10% duty cycle)	±40mA
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
16-Pin Plastic Dip	842mW
16-Pin Narrow SO	696mW
16-Pin QSOP	667mW
16-Pin TSSOP	457mW
Derates above +70°C	
16-Pin Plastic Dip	10.53mW/°C
16-Pin Narrow SO	8.7mW/°C
16-Pin QSOP	8.3mW/°C
16-Pin TSSOP	6.7mW/°C

Note 1: Voltages exceeding V_{CC} or V_{EE} on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

II. Manufacturing Information

A. Description/Function: Low-Voltage, CMOS Analog Switch

B. Process: S3 (SG3) - Standard 3 micron silicon gate CMOS

C. Number of Device Transistors: 219

D. Fabrication Location: California or Oregon, USA

E. Assembly Location: Malaysia, Philippines, Thailand, Korea

F. Date of Initial Production: January, 1998

III. Packaging Information

A. Package Type:	**16 Lead PDIP**	**16 Lead NSO**	**16 Lead QSOP**	**16 Lead TSSOP**
B. Lead Frame:	Copper	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)	Gold (1.0 mil dia)	Gold (1.0 mil dia)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1201-0039	05-1201-0040	05-1201-0041	05-1201-0106
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0	Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 53 x 69 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 3 microns (as drawn)

F. Minimum Metal Spacing: 3 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83 \text{ (Chi square value for MTTF upper limit)}}{192 \times 4389 \times 80 \times 2}$$

(192 × 4389 × 80 × 2: Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.57 \times 10^{-9}$ $\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5145) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1L**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AH14-1 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1

Reliability Evaluation Test Results

MAX4582xxE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	PDIP NSO QSOP TSSOP	260 1035 140 111	0 1 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the package.
Note 2: Generic process/package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

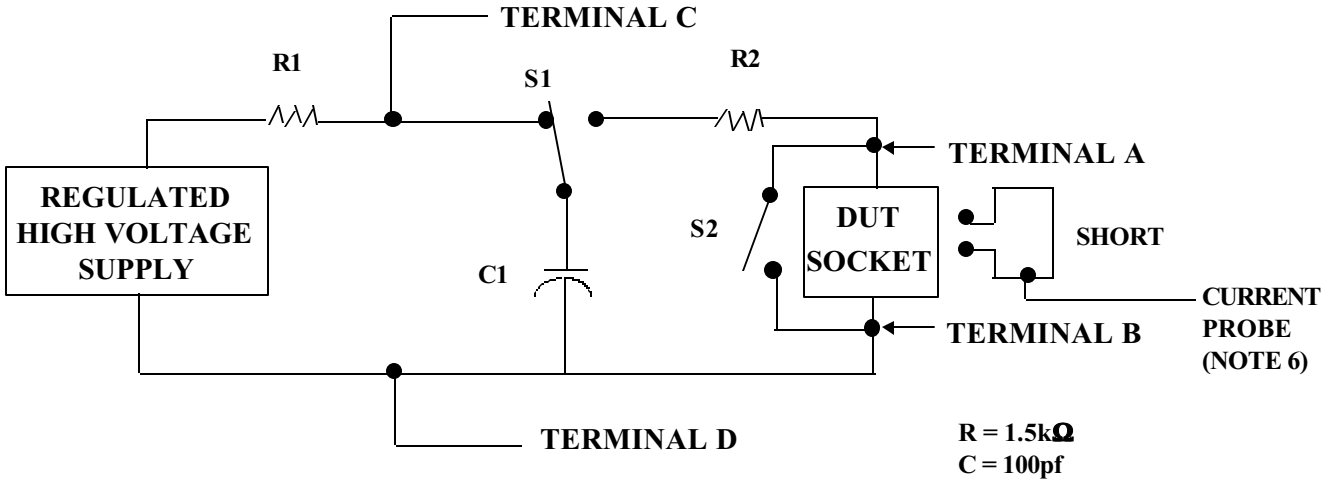
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

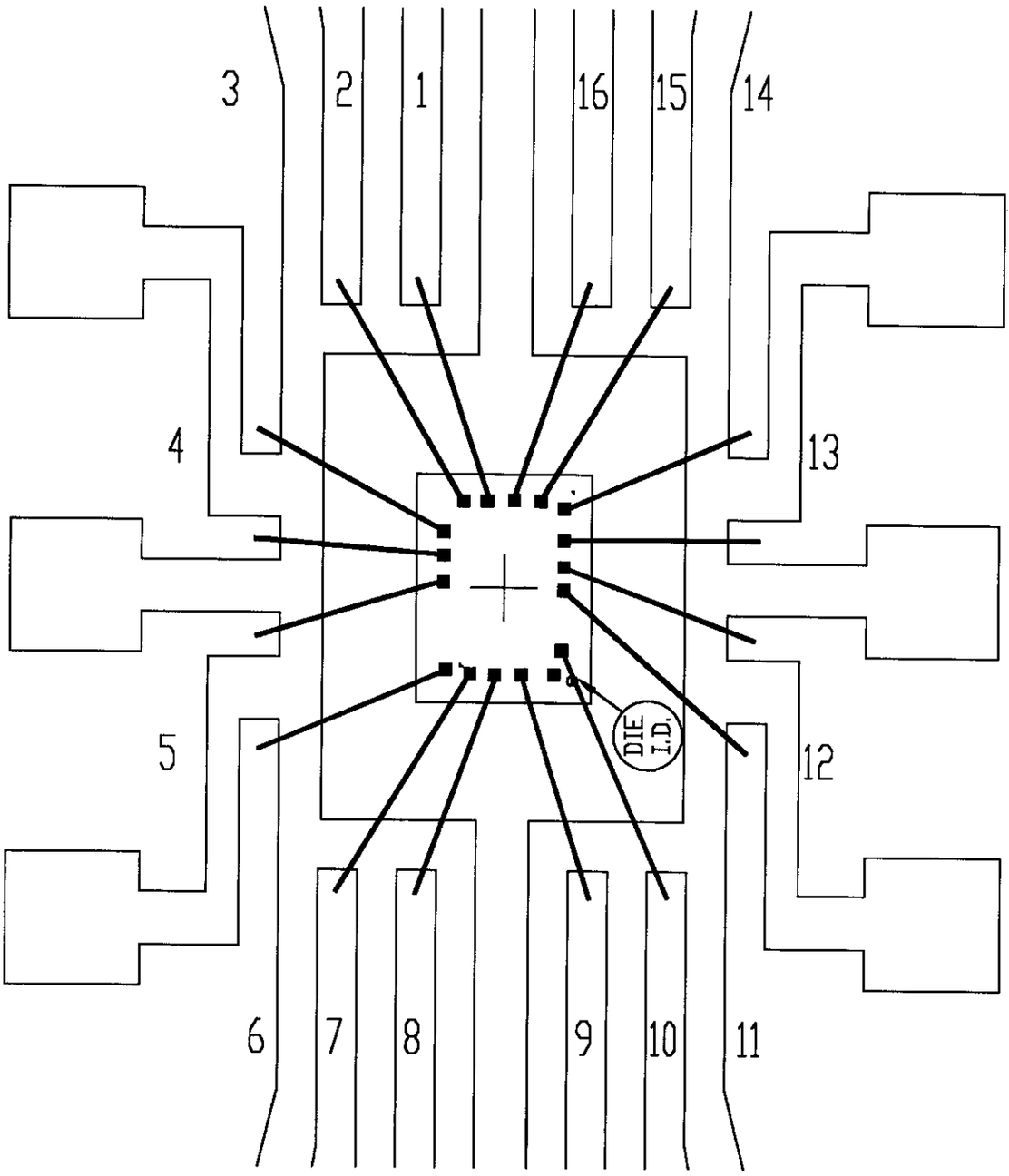
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

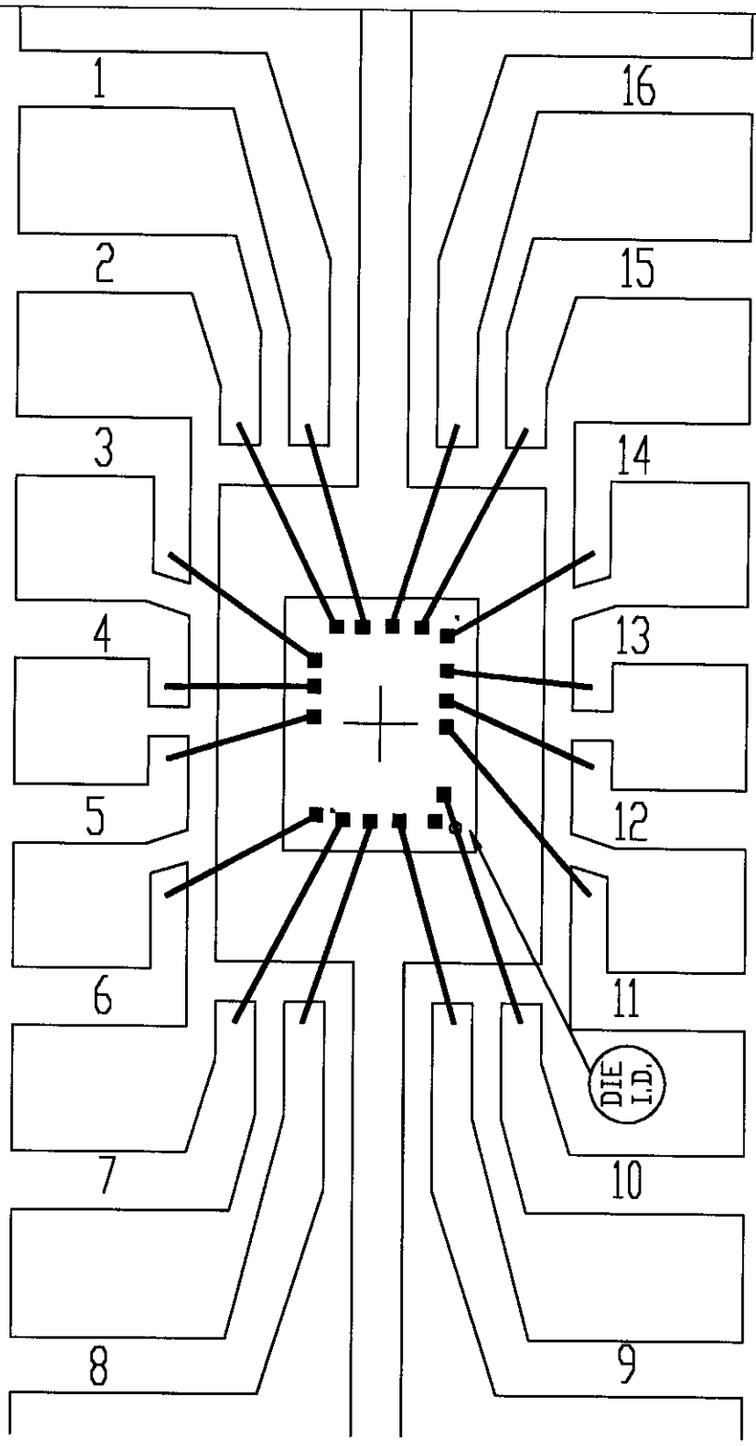
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

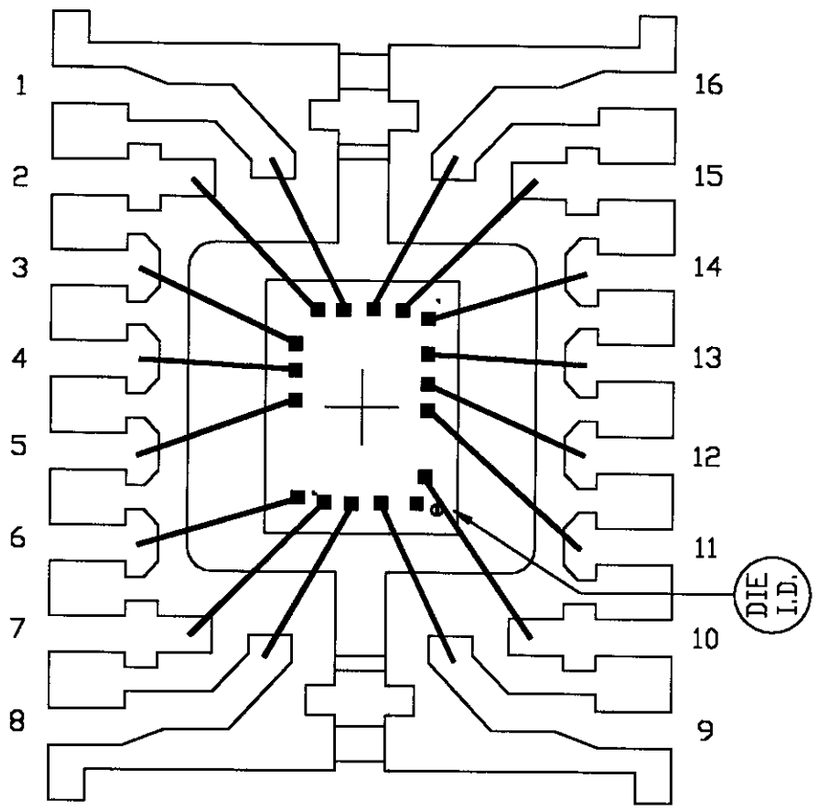




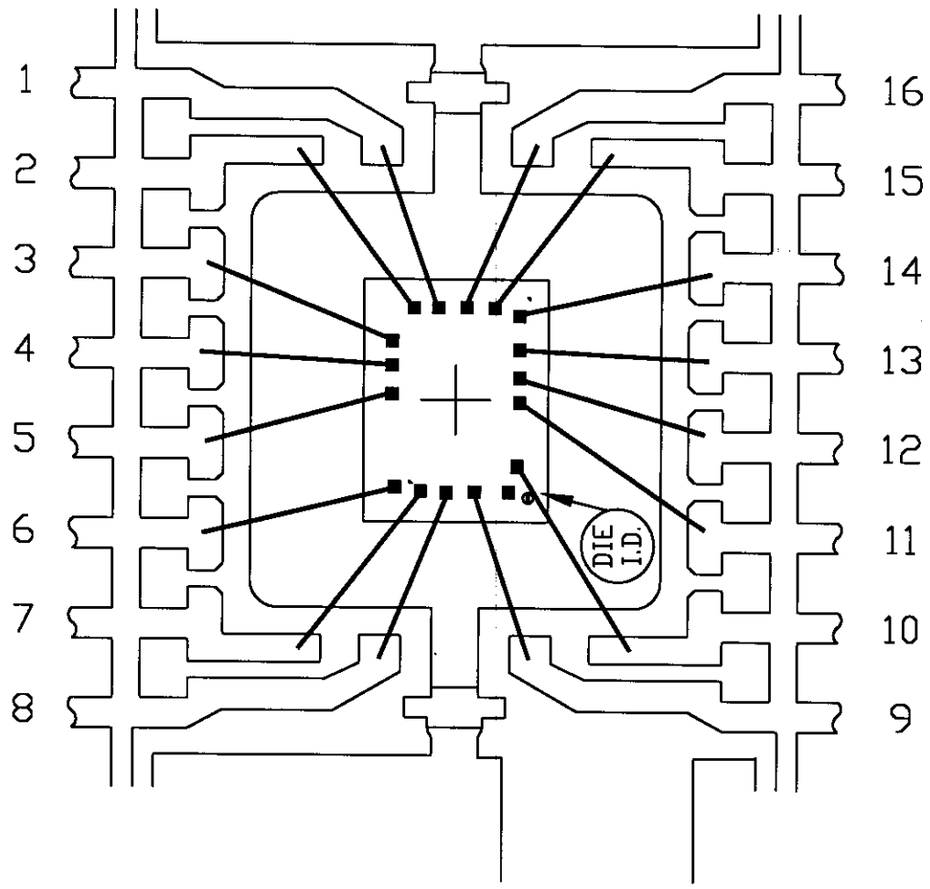
PKG.CODE: P16-1		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 110 X 140	PKG.		10/6/97	BUILDSHEET NUMBER: 05-1201-0039	REV.: A
	DESIGN	SR	10-2-97		



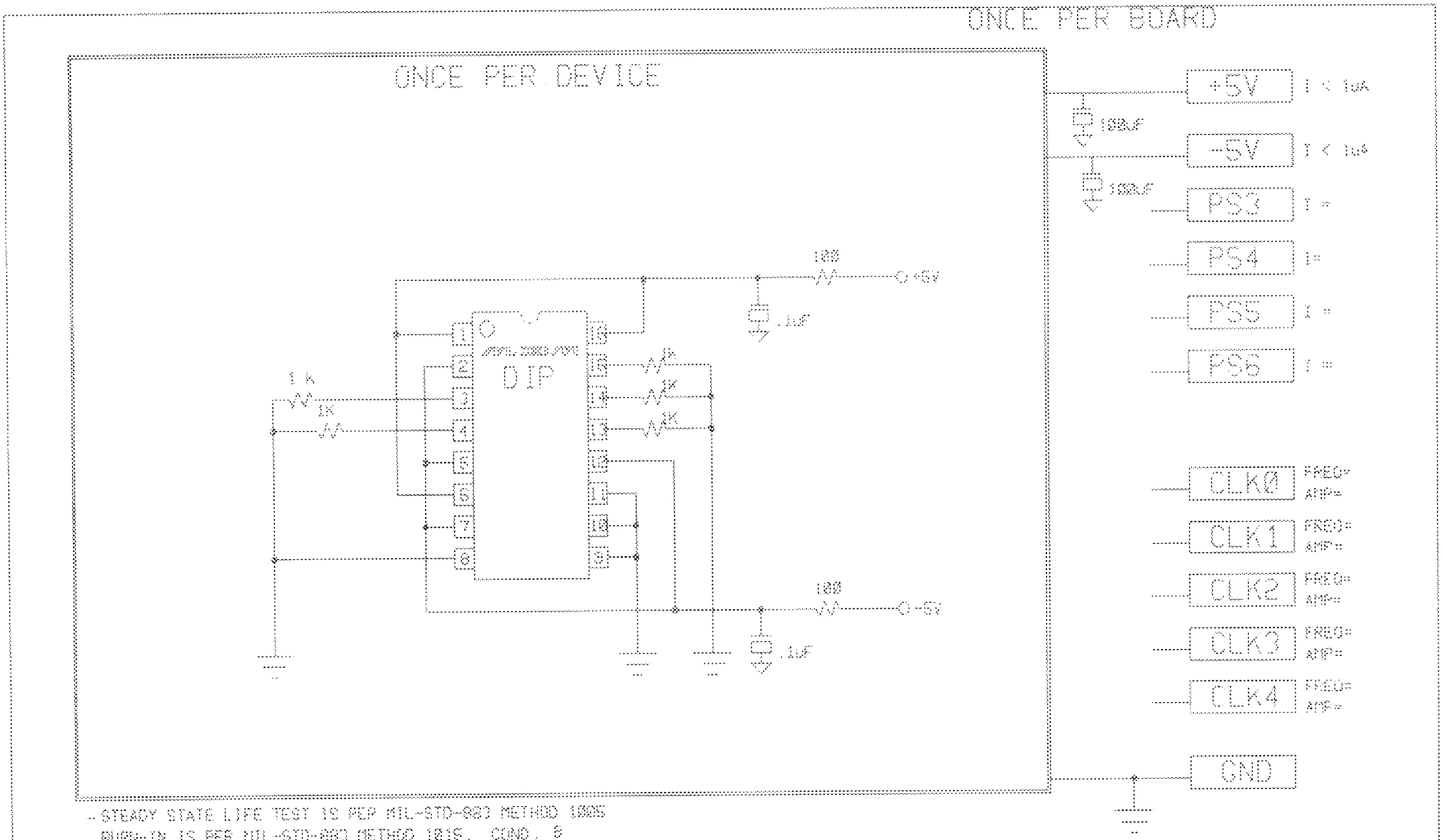
PKG.CODE: S16-2		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 90 X 130	PKG.		10/6/97	BUILDSHEET NUMBER: 05-1201-0040
	DESIGN		10-7-97	REV.: A



PKG.CODE: E16-4		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 96X90	PKG.		10/6/97	BUILDSHEET NUMBER: 05-1201-0041 REV.: A
	DESIGN	S.R	10-2-97	



PKG.CODE: U16-2		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 118X118	PKG.		4/21/99	BUILDSHEET NUMBER: 05-1201-0106	REV.: A
	DESIGN		4/23/99		



- STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005
- BURN-IN IS PER MIL-STD-883 METHOD 1015, COND. B

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR [X] COMMERCIAL
   [X] MR/883

SPEC. NO. 06-5145 REV: A

DATE: 9/21/95

DRAWN BY: R. TARIGA

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE(S):

MAX4051/52/53